Claims

[c1] What is claimed is:

1.A charge pump circuit for reducing capacitance in a loop filter of a phase locked loop, the loop filter comprising a resistor electrically connected to the charge pump circuit at an output node and a capacitor being electrically connected to the resistor at an intermediate node, the charge pump circuit comprising:

a first input current source electrically connected to a first node of the charge pump circuit for supplying a first current to the charge pump circuit, the first current being equal to a predetermined amount of current multiplied by a first factor;

a second input current source electrically connected to a second node of the charge pump circuit for supplying a second current to the charge pump circuit, the second current being equal to the predetermined amount of current multiplied by a second factor;

a first output current source electrically connected to a third node of the charge pump circuit for receiving the first current from the charge pump circuit;

a second output current source electrically connected to a fourth node of the charge pump circuit for receiving the second current from the charge pump circuit;

a plurality of up pulse switches controlled by an up pulse control signal for controlling current flow such that in a charging mode of the charge pump circuit, a sum of the first current and the second current flows from the first node through the output node and through the resistor to the intermediate node, the first current flows from the intermediate node to the third node and flows out through the first output current source, and the second current flows from the intermediate node through the capacitor for charging the capacitor; and

a plurality of down pulse switches controlled by a down pulse control signal for controlling current flow such that in a discharging mode of the charge pump circuit, the first current flows from the first node to the intermediate node, the second current flows from the capacitor to the intermediate node for discharging the capacitor, and the sum of the first current and the second

current flows from the intermediate node through the output node, the resistor, and the third node before flowing out through the first and second output current sources.

[c2] 2.The charge pump circuit of claim 1 wherein the plurality of up pulse switches comprises a first up pulse switch, a second up pulse switch, and a third up pulse switch, and the first up pulse switch is connected between the second node and the first node, the second up pulse switch is connected between the first node and the output node, and the third up pulse switch is connected between the intermediate node and the third node.

[c3] 3.The charge pump circuit of claim 2 wherein the plurality of down pulse switches comprises a first down pulse switch, a second down pulse switch, and a third down pulse switch, and the first down pulse switch is connected between the first node and the intermediate node, the second down pulse switch is connected between the output node and the third node, and the third down pulse switch is connected between the third node and the fourth node.

[c4] 4.The charge pump circuit of claim 3 wherein when the up pulse control signal is active and the charge pump circuit is in the charging mode, the first, second, and third up pulse switches close and the first, second, and third down pulse switches open.

[c5] 5.The charge pump circuit of claim 3 wherein when the down pulse control signal is active and the charge pump circuit is in the discharging mode, the first, second, and third down pulse switches close and the first, second, and third up pulse switches open.

[c6] 6.The charge pump circuit of claim 1 wherein the first and second factors are values less than one, and a sum of the first and second factors equals to one.

[c7] 7.The charge pump circuit of claim 6 wherein the second factor is less than the first factor.

[c8] 8.The charge pump circuit of claim 1 wherein the up pulse switches and the down pulse switches are transistors.

[c9] 9.A method of reducing capacitance in a loop filter of a phase locked loop, the loop filter comprising a resistor electrically connected to a charge pump circuit at an output node and a capacitor being electrically connected to the resistor at an intermediate node, the method comprising:

providing a first input current source electrically connected to a first node of the charge pump circuit for supplying a first current to the charge pump circuit, the first current being equal to a predetermined amount of current multiplied by a first factor;

providing a second input current source electrically connected to a second node of the charge pump circuit for supplying a second current to the charge pump circuit, the second current being equal to the predetermined amount of current multiplied by a second factor;

providing a first output current source electrically connected to a third node of the charge pump circuit for receiving the first current from the charge pump circuit;

providing a second output current source electrically connected to a fourth node of the charge pump circuit for receiving the second current from the charge pump circuit;

controlling a plurality of up pulse switches with an up pulse control signal for controlling current flow such that in a charging mode of the charge pump circuit, a sum of the first current and the second current flows from the first node through the output node and through the resistor to the intermediate node, the first current flows from the intermediate node to the third node and flows out through the first output current source, and the second current flows from the intermediate node through the capacitor for charging the capacitor; and

controlling a plurality of down pulse switches with a down pulse control signal for controlling current flow such that in a discharging mode of the charge pump circuit, the first current flows from the first node to the intermediate node, the second current flows from the capacitor to the intermediate node for discharging the capacitor, and the sum of the first current and the second current flows from the intermediate node through the output node, the resistor, and the third node before flowing out through the first and second output

current sources.

[c10] 10.The method of claim 9 wherein the plurality of up pulse switches comprises a first up pulse switch, a second up pulse switch, and a third up pulse switch, and the first up pulse switch is connected between the second node and the first node, the second up pulse switch is connected between the first node and the output node, and the third up pulse switch is connected between the intermediate node and the third node.

[c11] 11.The method of claim 10 wherein the plurality of down pulse switches comprises a first down pulse switch, a second down pulse switch, and a third down pulse switch, and the first down pulse switch is connected between the first node and the intermediate node, the second down pulse switch is connected between the output node and the third node, and the third down pulse switch is connected between the third node and the fourth node.

[c12] 12.The method of claim 11 wherein when the up pulse control signal is active and the charge pump circuit is in the charging mode, the first, second, and third up pulse switches close and the first, second, and third down pulse switches open.

[c13] 13.The method of claim 11 wherein when the down pulse control signal is active and the charge pump circuit is in the discharging mode, the first, second, and third down pulse switches close and the first, second, and third up pulse switches open.

[c14] 14.The method of claim 9 wherein the first and second factors are values less than one, and a sum of the first and second factors equals to one.

[c15] 15.The method of claim 14 wherein the second factor is less than the first factor.

[c16] 16.The method of claim 9 wherein the up pulse switches and the down pulse switches are transistors.